CLAIMS

What is claimed is:

Sub C4

1. A circuit device comprising:

a first transistor including a first metal gate electrode overlying [a over] a first gate dielectric on a first area of a semiconductor substrate and having a work function corresponding to the work function of one of P-type silicon and N-type silicon; and

fig. 7

a second transistor complementary to the first transistor including a second metal gate electrode over a second gate dielectric on a second area of a semiconductor substrate and having a work function corresponding to the work function of the other one of P-type silicon and N-type silicon.

2. The integrated circuit device of claim 1, wherein the first metal gate electrode is one of a pure metal, a doped metal, and a metal alloy.

3. A method of forming a circuit device, comprising:

forming a gate dielectric overlying a region of a substrate;

depositing a metal layer over the gate dielectric; and

modifying the Fermi level of the metal layer.

4. The method of claim 3, further comprising the step of patterning the metal layer into a gate electrode.

5. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes chemically reacting the metal layer with a compound.

6. The method of claim 5, wherein the region of the substrate includes a first region and a second region, and prior to the step of modifying the first metal layer, the method further comprises the step of:

masking the metal layer over the second region.

7. The method of claim 6, wherein the masking step includes masking with an inert compound.

8. The method of claim 6, wherein the masking step includes masking with a masking compound that reacts with the metal layer over the second region to modify the Fermi level of the reaction product.

9. The method of claim 8, wherein the masking compound is polysilicon.

10. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes alloying the metal layer with one of a second metal layer and a silicon.

11. The method of claim 10, wherein the region of the substrate includes a first region and a second region, and the step of modifying the metal layer comprises modifying one of the first region and the second region.

12. The method of claim 11, wherein the step of alloying the metal layer includes alloying with a polysilicon.

13. The method of claim 3, wherein the step of modifying the Fermi level of the metal layer includes implanting an ion into the metal layer.

14. The method of claim 13, wherein the region of the substrate includes a first region and a second region, and the step of modifying the metal layer comprises modifying one of the first region and the second region.

15. The method of claim 14, wherein after the step of modifying the metal layer of one of the first region and the second region, the method comprises the step of modifying the other of the first region and the second region.

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